REMARKS

Applicant appreciates the Office Action of June 8, 2004. Applicant has amended a portion of the specification at page 11 as set out above to correct typographical errors. Applicant respectfully submits that the pending claims are patentable over the cited references for at least the reasons discussed herein. Accordingly, Applicant respectfully requests allowance of the pending claims in due course.

The 102 Rejections

Claims 1-4 and 47 stand rejected under 35 U.S.C. § 102 as being unpatentable over Applicant Admitted Prior Art (hereinafter "the AAPA"). Applicant respectfully submits that the AAPA neither discloses nor suggests many of the recitations of the pending claims. For example, Claim 1 recites:

> A phase changeable memory device comprising:
> an integrated circuit substrate;
> a first storage active region on the integrated circuit substrate having a first width;
> a second storage active region on the integrated circuit substrate having a second width; and
> **a transistor active region on the integrated circuit substrate between the first and second storage active regions, the first and seconds widths being less than a width of the transistor active region.**

Applicant respectfully submits that at least the highlighted portions of Claim 1 are neither disclosed nor suggested by the cited reference.

The Office Action states that the AAPA teaches all the recitations of Claim 1 of the present application. *See* Office Action, page 3. In particular, the Office Action states that phase changeable material pattern 40 of Figure 3 teaches the first and second storage active regions as recited in Claim 1 and that the active region 10 teaches the transistor active region as recited in Claim 1. As recited in the Background of the Invention:

> Referring now to Figure 3, a plan view illustrating a portion of a cell array of conventional phase changeable memory devices will be discussed. As illustrated in Figure 3, a plurality of active regions 10 are two-dimensionally disposed on an

> integrated circuit substrate. A plurality of gate lines 20 are disposed crossing over the active regions 10. The gate lines 20 correspond to word lines. **The active regions 10** are disposed beneath a plurality of gate lines 20, for example, two gate lines 20. As illustrated, **the active regions 10 are divided into three regions** by the plurality of gate lines 20. **A portion of the active region 10 between the plurality of gate lines 20 may correspond to a common drain region 11. Portions of the active region 10 on either side of the common drain region 11 may correspond to source regions 12 and 13.** The common drain region 11, one of the source regions 12 and 13 and the gate line 20 provide a transistor. In other words, each active region 10 includes two unit cells.
>
> The common drain region 11 is electrically connected to bit line 30 through bit line contact hole 25. A plurality of bit lines 30 cross over the gate lines 20. A phase changeable material pattern 40 is disposed over the source region. **The phase changeable material pattern 40 is electrically connected to the source regions 12 and 13 under the phase changeable material pattern 40, through a heater plug (not shown) in a contact hole 35.** The phase changeable material pattern 40 is electrically connected to the plate electrode (not shown) over the phase changeable memory device.
>
> **The phase changeable material pattern 40 may be formed of GTS and the heater plug may be formed of titanium nitride (TiN).** ...

See Background of the invention, page 2, line 28 to page 3, line 14 (emphasis added). Thus, the phase changeable material pattern 40 discussed in the background of the invention is not a storage active region as recited in Claim 1 and the active region 10 is not the transistor active region recited in Claim 1. As recited in the portion of the background of the invention set out above, the active regions 10 are divided into three regions, a common drain region 11 and first and second regions 12 and 13, which may correspond to the transistor active region and the first and second source regions, respectively, as recited in Claim 1 in some embodiments of the present invention. Accordingly, as illustrated in Figure 3, the widths (parallel to the gate lines 20) of the first and second source regions 12 and 13 (first and second storage active regions) is not less than a width of the common drain region 11 (the transistor active region). In fact, the widths of the first and second source regions 12 and 13 are equal to the width of the common drain region 11.

In contrast, as illustrated in Figure 5 of the present invention, the first and second storage active regions 102 and 103 have widths k (parallel to the gate lines 117) and the transistor active region 101 has a width W. As is clearly illustrated in Figure 5, the widths k

of the first and second active regions 102 and 103 are less than the width W of the transistor active region 101. Nothing in the AAPA discloses or suggests widths of the first and second storage active regions being less than a width of transistor active region as recited in Claim 1 of the present invention.

The Office Action further asserts that the AAPA discloses all of the recitations of Claim 47. *See* Office Action, page 4. Applicant respectfully disagrees. In particular, Claim 47 recites:

> A phase changeable memory device comprising:
> an integrated circuit substrate;
> a first storage active region on the integrated circuit substrate having a first cross sectional area;
> a second storage active region on the integrated circuit substrate having a second cross sectional area; and
> **a transistor active region on the integrated circuit substrate between the first and second storage active regions, the first and seconds cross sectional areas being less than a cross sectional area of the transistor active region.**

Applicant submits that at least the highlighted portions of Claim 47 are neither disclosed nor suggested by the cited references. As illustrated in Figure 3, the first and second source regions 12 and 13 are approximately the same size as the common drain region 11 and, thus, by definition the cross sectional areas of the source regions 12 and 13 cannot be less than the cross sectional area of the common drain region 11. Thus, for at least these reasons, nothing in the AAPA discloses or suggests the highlighted recitations of Claim 47.

Accordingly, for at least the reasons discussed above, Applicant submits that independent Claims 1 and 47 are patentable over the cited references. Furthermore, the dependent Claims are patentable at least per the patentability of the independent base claims from which they depend. Thus, the pending claims are in condition for allowance, which is respectfully requested in due course.

Many of the Dependent Claims are Independently Patentable

Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view of United States Patent No. 6,030,548 to Kuriyama. Claims 6, 7, 16 and 17

stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view of United States Patent No. 6,545,903 to Wu. Claims 8, 9, 12, 13, 18 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view of Wu and in further view of U.S. Patent No. 5,952,671 to Reinburg. Claims 14, 15, 22 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view of Wu and in further view of Brassington.

As discussed above, the dependent claims are patentable over the cited references at least per the patentability of the independent base claims from which they depend. Many of the dependent claims are also separately patentable.

For example, Claim 2 recites "wherein the first width is equal to the second width and the first and second widths are about half of the width of the transistor active region." As discussed above, the first and second source regions 12 and 13 have approximately the same width as the common drain region 11 and, therefore, cannot each have a width equal to about half the width of the common drain region 11 as recited in Claim 2. Accordingly, Claim 2 is separately patentable over the cited references for at least these additional reasons.

By way of further example, Claim 3 recites:

> A device according to Claim 1 further comprising a plurality of gate lines defining a plurality of rows of the phase changeable memory device, **wherein a plurality of the first and second storage active regions are disposed alternately along the rows in a region between first and second gate lines of the plurality of gate lines** and wherein the widths of the first and second storage active regions and the width of the transistor active region are parallel to the plurality of gate lines.

As illustrated in Figure 3, a plurality of first source regions 12 are disposed in a line parallel to the gate line 20 and a plurality of second source regions 13 are disposed in a line parallel to the gate line and the line of first source regions 12. In contrast, as illustrated in Figure 5, in embodiments of the present invention a plurality of first and second storage active regions are **alternately** disposed in a straight line parallel to the gate line 117. Nothing in the cited references discloses or suggests having a line alternating first and second storage active regions parallel to the gate line as recited in Claim 3. Accordingly, Claim 3 is separately patentable over the cited references for at least these additional reasons.

By way of final example, Claim 4 recites:

> A device according to Claim 1 wherein the transistor active region comprises first and second sidewalls extending from a first end of the transistor active region to a second end of the transistor active region, wherein the first storage active region **protrudes from the first sidewall of the transistor active region at the first end of the transistor active region and wherein the second storage region protrudes from the second sidewall of the transistor active region at the second end of the transistor active region.**

As illustrated in Figure 3, the first and second source regions 12 and 13 do not protrude out of **different ends** of the common drain region 11 as recited in Claim 4. Accordingly, Claim 4 is separately patentable over the cited references for at least these additional reasons.

CONCLUSION

Applicant respectfully submits that the pending claims are patentable over the cited reference for at least the reasons stated herein. Accordingly, Applicant submits that the pending claims are in condition for allowance, which is respectfully requested in due course. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

It is not believed that an extension of time and/or additional fee(s)-including fees for net addition of claims-are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to our Deposit Account No. 50-0220.

Respectfully submitted,

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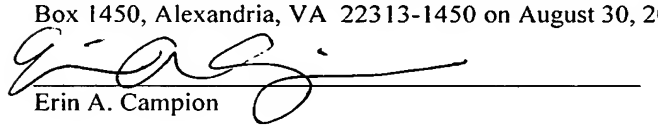

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